## IN THE CLAIMS

Please delete claims 1-11 and add new claims 12-38 as follows:

12. A hybrid active electronic and optical circuit integrated within a Silicon-On-Insulator (SOI) wafer, the SOI wafer including an insulator layer and an upper silicon layer, the hybrid active electronic and optical circuit comprising:

a waveguide located within the upper silicon layer for receiving light;

an active electronic circuit positioned proximate the waveguide, wherein a flow of light through the waveguide can be altered depending on a property of the active electronic circuit;

an evanescent coupling region at least partially located within the upper silicon layer, the evanescent coupling region optically couples the light coupling portion to the waveguide, light emitted from the light coupling portion can pass via the evanescent coupling region to the waveguide at a suitable angle; and

a light deflector at least partially located in the upper silicon layer, the light deflector is configured to deflect light impinging at the suitable incident angle to a suitable mode angle wherein light deflected by the light deflector enters the waveguide.

13. The hybrid active electronic and optical circuit of claim 12, wherein the evanescent coupling region includes a tapered gap portion.

14. The hybrid active electronic and optical circuit of claim 13, wherein the tapered gap portion enhances coupling efficiency.

15. The hybrid active electronic and optical circuit of claim 12, wherein the evanescent coupling region includes a substantially constant thickness gap portion.

16. The hybrid active electronic and optical circuit of claim 12, wherein the evanescent coupling region is at least partially formed using an optically clear adhesive.

17. The hybrid active electronic and optical circuit of claim 12, wherein the evanescent coupling region is at least partially formed from air.

18. The hybrid active electronic and optical circuit of claim 12, further including at least one optical device, wherein altering an electric voltage applied to the active electronic circuit affects a free carrier distribution in a region of the at least one optical device, and thereby changes an effective mode index of the at least one optical device.

19. The hybrid active electronic and optical circuit of claim 12, wherein the evanescent coupling region is at least partially formed from an optically clean polymer.

20. The hybrid active electronic and optical circuit of claim 12, wherein the evanescent coupling region has a thickness of less than 0.5μ.

21. The hybrid active electronic and optical circuit of claim 12, wherein the evanescent coupling region includes a waveguide prism.

22. The hybrid active electronic and optical circuit of claim 13, wherein the evanescent coupling region includes a waveguide prism.

23. The hybrid active electronic and optical circuit of claim 15, wherein the evanescent coupling region includes a waveguide prism.

24. The hybrid active electronic and optical circuit of claim 12, wherein the evanescent coupling region includes a waveguide grating.

25. The hybrid active electronic and optical circuit of claim 13, wherein the evanescent coupling region includes a waveguide grating.

26. The hybrid active electronic and optical circuit of claim 15, wherein the evanescent coupling region includes a waveguide grating.

27. The hybrid active electronic and optical circuit of claim 12, wherein the hybrid active electronic and optical circuit includes a focusing mirror.

28. The hybrid active electronic and optical circuit of claim 12, wherein the hybrid active electronic and optical circuit includes an input/output coupler that couples light into or out of the waveguide.

29. The hybrid active electronic and optical circuit of claim 12, wherein the hybrid active

electronic and optical circuit includes a Fabry-Perot cavity.

30. The hybrid active electronic and optical circuit of claim 12, wherein the hybrid active electronic and optical circuit includes a wavelength division multiplexer modulator.

31. The hybrid active electronic and optical circuit of claim 12, wherein the hybrid active electronic and optical circuit includes a diode.

32. The hybrid active electronic and optical circuit of claim 12, wherein the hybrid active electronic and optical circuit includes a transistor.

33. The hybrid active electronic and optical circuit of claim 12, wherein the waveguide is at least partially formed using a plurality of electric insulator strips.

34. The hybrid active electronic and optical circuit of claim 12, wherein the light deflector includes a waveguide grating.

35. The hybrid active electronic and optical circuit of claim 12, wherein the light deflector includes a waveguide prism.

36. The hybrid active electronic and optical circuit of claim 12, wherein the light deflector includes a lens.

37. The hybrid active electronic and optical circuit of claim 12, wherein the hybrid circuit includes one from the group of a p-n device, a field plated device, a Schottky device, a MOSCAP, and a MOSFET.

38. A hybrid active electronic and optical circuit integrated within a wafer, the wafer including an insulator layer and an upper silicon layer, the hybrid active electronic and optical circuit comprising:

a waveguide located within the upper silicon layer for receiving light;

an active electronic circuit positioned proximate the waveguide, wherein a flow of light through the waveguide can be altered depending on a property of the active electronic circuit;

an evanescent coupling region at least partially located within the upper silicon layer, the evanescent coupling region optically couples the light coupling portion to the waveguide, light emitted from the light coupling portion can pass via the evanescent coupling region to the waveguide at a suitable angle; and

a light deflector at least partially located in the upper silicon layer, the light deflector is configured to deflect light impinging at the suitable incident angle to a suitable mode angle $\theta_M$ wherein light deflected by the light deflector enters the waveguide.

## IN THE DRAWINGS

Applicant respectfully requests the Examiner's approval of the proposed changes to the drawing figures 5, 13, 20, 21, 22, 30, 47, 51, 52, 59, 60, 68A, 68B, 68C, 68D, 73, 74, 75, 76, 77, 78, 82, 83 and 88 in the request for Approval of Drawing Changes filed concurrently herewith.